

V1 38 Way Varelco Pinout

82E57 Bargraph Logic Card
82E59 Bargraph Scale Card
82E83 Bargraph Scale Card

No | Description

1	Cathode 4, Bargraph pin 9
2	Cathode 2, Bargraph pin 8
3	Cathode 3, Bargraph pin 7
4	Reset Cathode, Bargraph pin 4
5	Cathode 0, Bargraph pin 3
6	Cathode 1, Bargraph pin 2
7	not used
8	Keep Alive Anode, Bargraph pin 5
9	Left Anode, Bargraph pin 1
10	Right Anode, Bargraph pin 10
11	not used
12	Keep Alive Cathode, Bargraph pin 6
13	not used
14	0 Volts
15	Right Signal Switch
16	Analog Ramp
17	VU Ballistics
18	PPM Ballistics
19	Channel Relay
20	Spectra Relay
21	Spectra Signal Bus
22	A=B Test Point
23	Left Signal Switch
24	--
25	
26	
27	- not used
28	
29	
30	
31	-
32	+13 Volts
33	+20 Volts
34	-20 Volts
35	Spectra Markers
36	VU Scale
37	VU Scale
38	PPM Scale

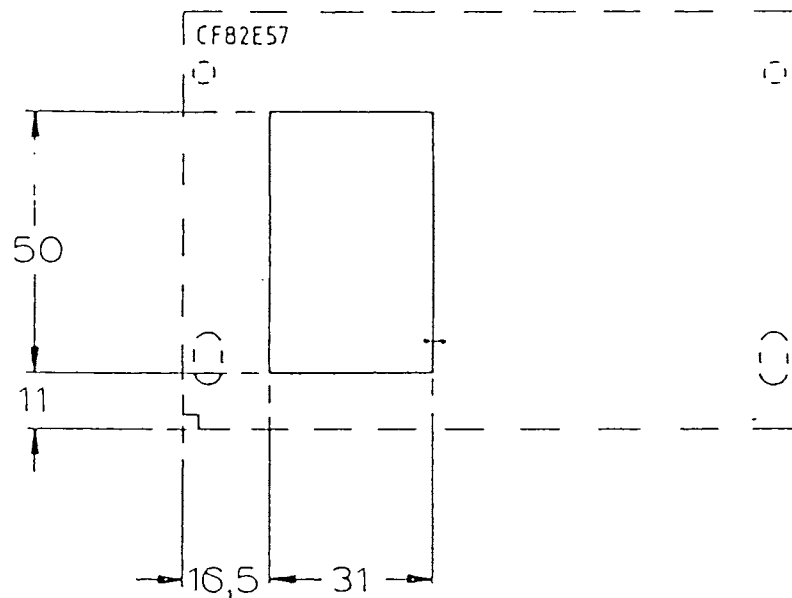
S65E 40 Way Ribbon

82E57 Bargraph Logic Card
82E58 Bargraph Mother Card

No | Description

1	0 Volts
2	+20 Volts
3	0 Volts
4	-20 Volts
5	Display Store R
6	+13 Volts
7	Display Store L
8	Display Signal L
9	Display Signal R
10	Anode Enable R
11	Anode Enable L
12	Store Enable
13	Clear
14	MSB Digital Ramp
15	6
16	5
17	4
18	3
19	2
20	1
21	LSB
22	Spectra Signal Bus
23	Spectra Relay
24	Channel Relay
25	PPM Ballistics
26	VU Ballistics
27	Analog Ramp
28	PPM Scale
29	Spectra Markers
30	VU Scale
31	spare
32	spare
33	+263 Volts
34	+263 Volts
35	Cathode 1 H.T.
36	Cathode 0 H.T.
37	Reset Cathode
38	Cathode 3 H.T.
39	Cathode 2 H.T.
40	Cathode 4 H.T.

T82057.50
12 June 81

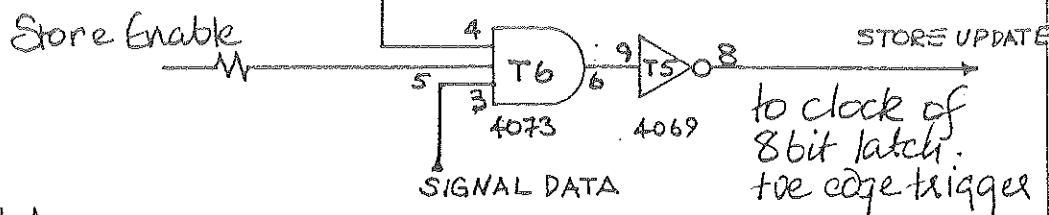


ALL DIMENSIONS ARE IN MILLIMETRES.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
-	A	NEW DRG. ADDED.	3-7-81	J. EVINS.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± ±	CONTRACT NO.	Solid State Logic Stonesfield · Oxford · England		
MATERIAL 1/16" P.C.B. BOARD. FINISH CLAD WITH SOLDER RESIST.	APPROVALS	DATE	DRG. SHOWING SIZE & POSITION OF 82E57 H.T. SCREEN.	
	DRAWN J. EVINS.	3-7-81		
	CHECKED J. EVINS.	3-7-81	SIZE A3	FSCM NO.
DO NOT SCALE DRAWING	ISSUED <i>[Signature]</i>	3-7-81	DWG. NO. 82E57	REV.
		SCALE 1:1	SHEET 1 OF 1	

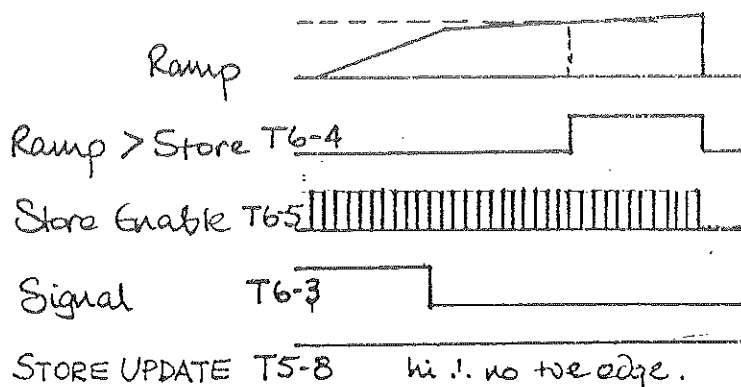
Store Clock; Explain:



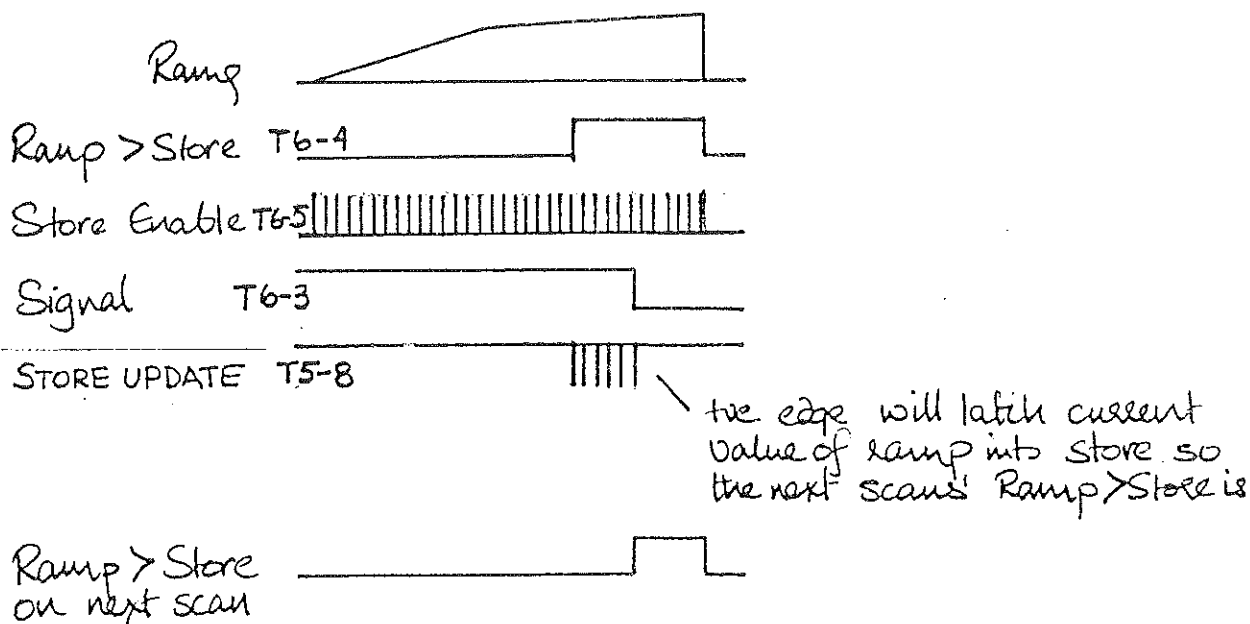
Possible states;

① Not Storing: The Store Enable low, $\therefore$ output of 4073 low
 $\therefore$ output of 4069 hi,
 $\therefore$ no +ve edge.

② Storing; with store bigger than signal;



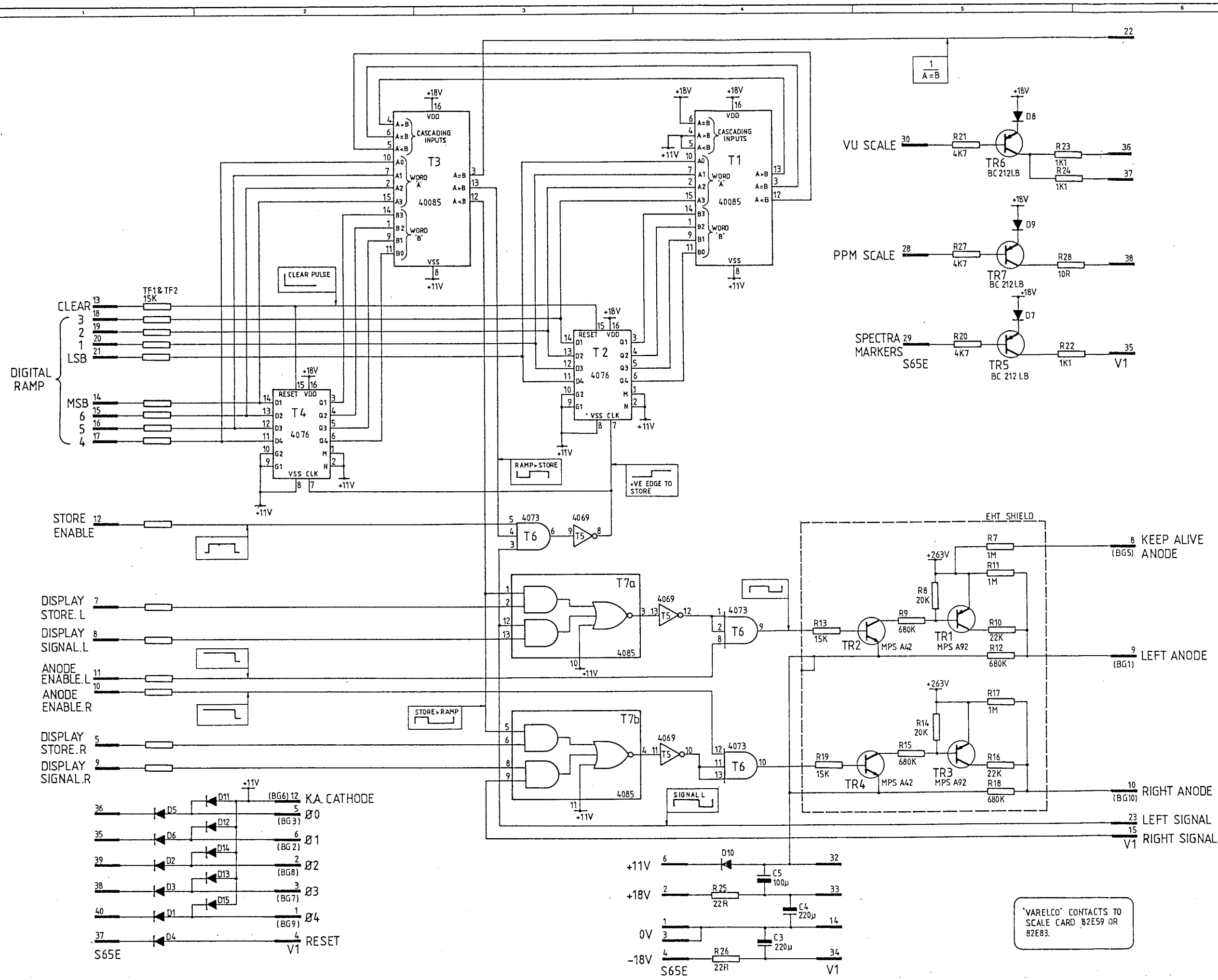
③ Storing; with signal bigger than store, $\therefore$ latch clock is required at -ve edge of signal;



SOLID STATE LOGIC STONSFIELD OXFORD ENGLAND		MODEL:- DRAWING No:-	
82657		-401	
LIMITS UNLESS STATED: TOL: 1/100 ... 1/1000 ... 1/10000 ANGLES: 1°		SCALE	
MATERIAL:-		FINISH:-	
IF IN DOUBT ASK		DO NOT SCALE DRAWING	
THIS DRAWING, IN ADDITION TO SOLID STATE LOGIC AND ITS ISSUING OFFICE, IS TO BE KEPT IN THE OFFICE OF THE CUSTOMER FOR THE PURPOSE OF THE CONTRACT IN WRITING OF SOLID STATE LOGIC.		DATE	

MY 112548 R

17 JUN 81 4
DATE REV
MODIFICATION



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Rev.	Issue	Chkd	Details
4	a	681	JK.
5	a	12-81	R8-9-14-15 CHANGED.
6	a	2-82	C1,C2 DELETED.
7	a	11-82	R22-23-24 CHANGED.
8	a	2-83	R22-23-24 CHANGED.
9	a	4-84	DIODES D11-16 ADDED.
10	a	10-85	DIODES DELETED.
11	a	11-85	D8-10 ADDED. C3-5 AMENDED.
11	b	DM Feb 86	D8-10 RENUMBERED TO D13-15.
11	c	AM Mar 86	REDRAWN
11	d	AM June 86	POWER TO ICs

Title		BARGRAPH METER LOGIC CARD
Drg. No.		T82057-71
Solid State Logic		12-36